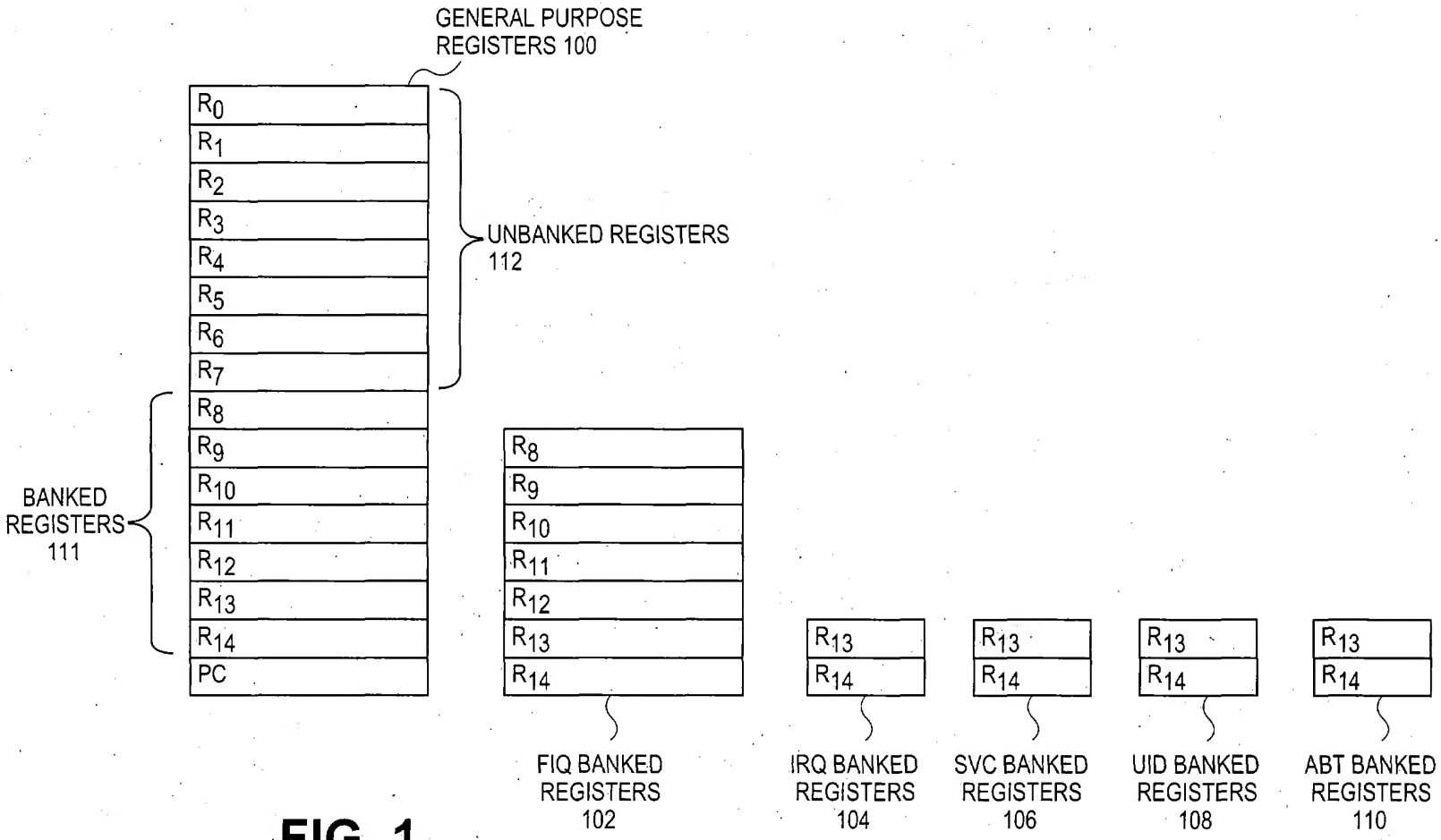

FIG. 1
(PRIOR ART)

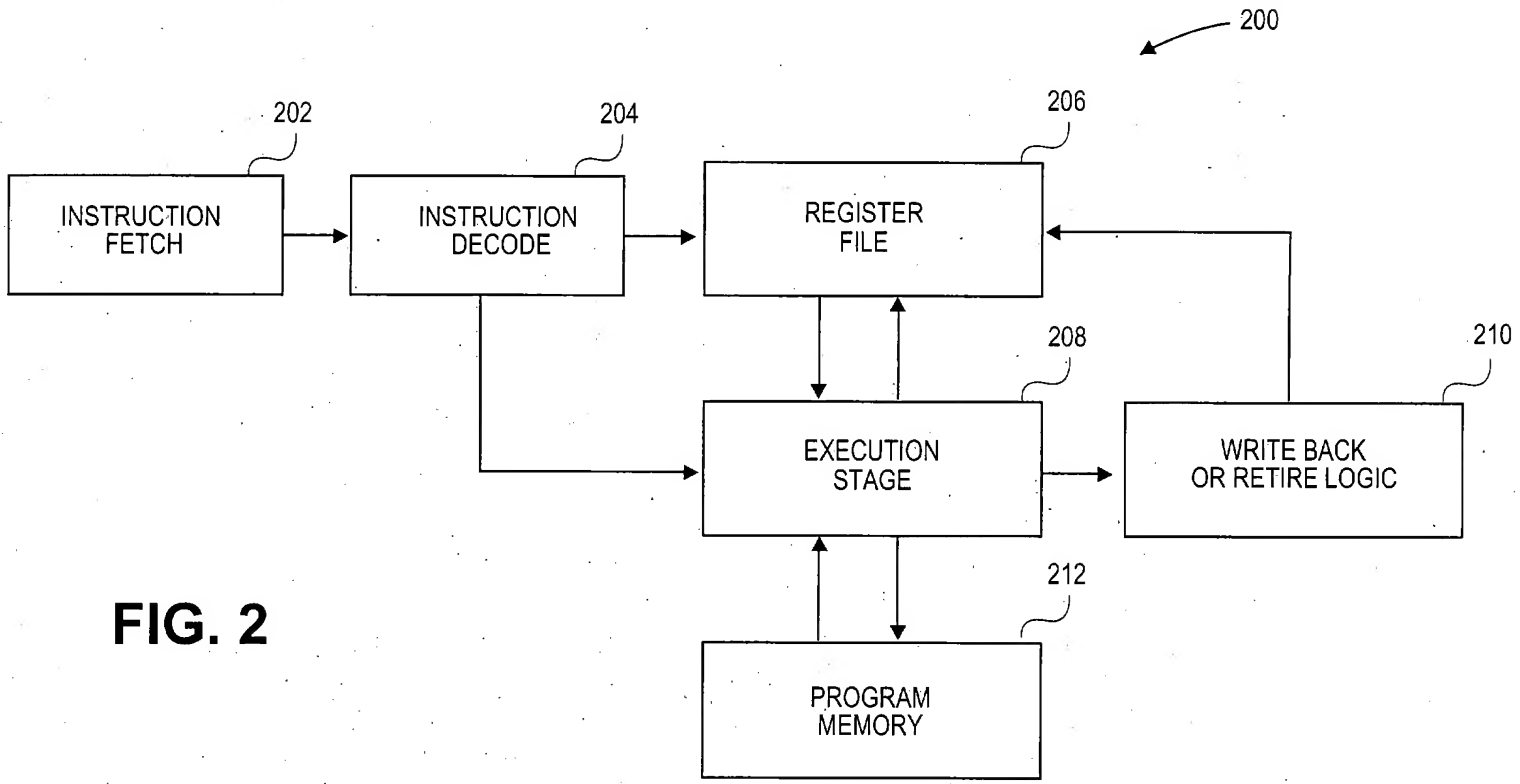
200
202
INSTRUCTION FETCH
204
INSTRUCTION DECODE
206
REGISTER FILE
208
EXECUTION STAGE
210
WRITE BACK OR RETIRE LOGIC
212
PROGRAM MEMORY

FIG. 2

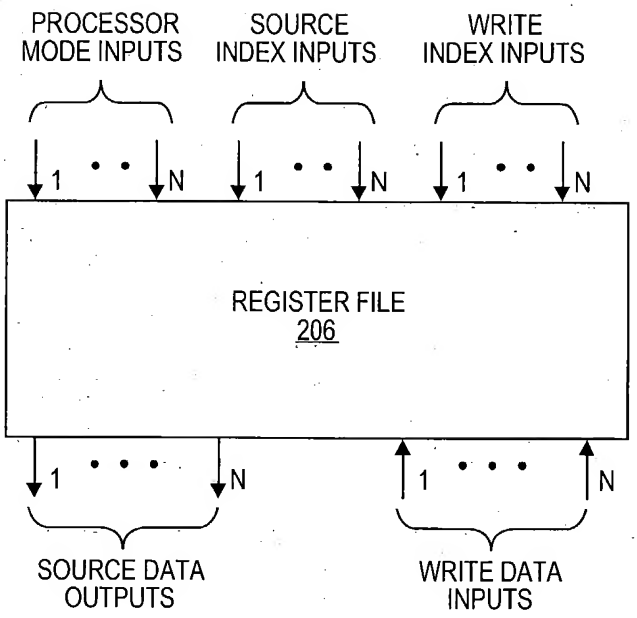
PROCESSOR MODE INPUTS
SOURCE INDEX INPUTS
WRITE INDEX INPUTS
1
N
1
N
1
N
REGISTER FILE
206
1
N
1
N
SOURCE DATA OUTPUTS
WRITE DATA INPUTS

FIG. 3

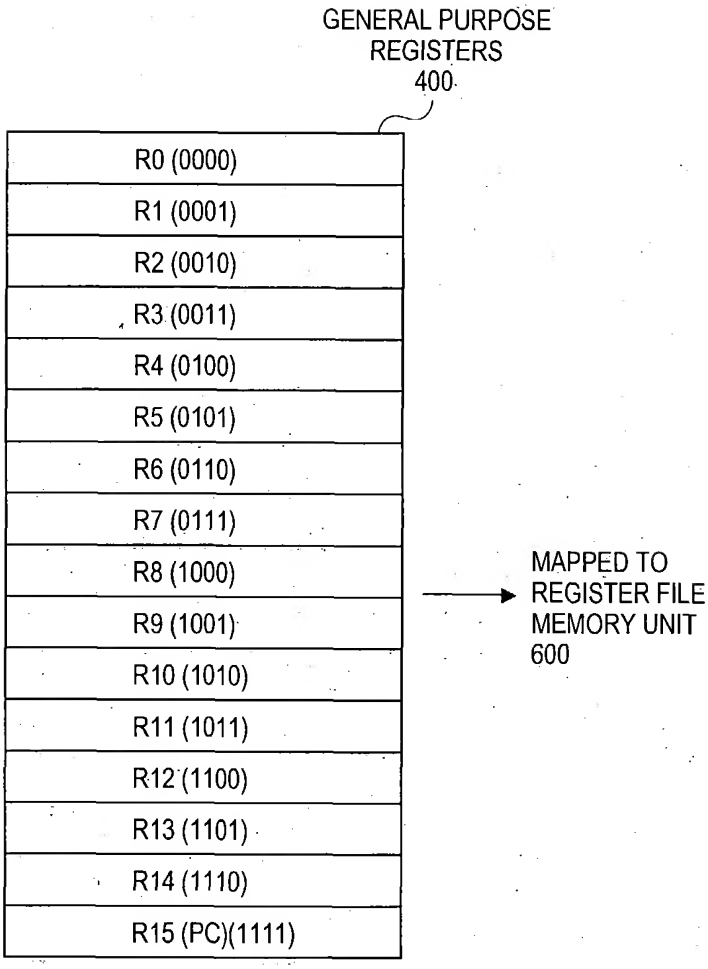
GENERAL PURPOSE
REGISTERS
400
R0 (0000)
R1 (0001)
R2 (0010)
R3 (0011)
R4 (0100)
R5 (0101)
R6 (0110)
R7 (0111)
R8 (1000)
R9 (1001)
R10 (1010)
R11 (1011)
R12 (1100)
R13 (1101)
R14 (1110)
R15 (PC)(1111)
MAPPED TO
REGISTER FILE
MEMORY UNIT
600

FIG. 4

MEMORY MAP 500

Address	Processor Mode	Encoded Address
R0 (0000)	ALL	00000
R1 (0001)	ALL	00001
R2 (0010)	ALL	00010
R3 (0011)	ALL	00011
R4 (0100)	ALL	00100
R5 (0101)	ALL	00101
R6 (0110)	ALL	00110
R7 (0111)	ALL	00111
R8 (1000)	FIQ	01000
R9 (1001)	FIQ	01001
R10 (1010)	FIQ	01010
R11 (1011)	FIQ	01011
R12 (1100)	FIQ	01100
R13 (1101)	FIQ	01101
R14 (1110)	FIQ	01110
Reserved (1111)	ALL	01111
R14 (1110)	IRQ	10000
R13 (1100)	IRQ	10001
R14 (1110)	SVC	10010
R13 (1100)	SVC	10011
R14 (1110)	UND	10100
R13 (1100)	UND	10101
R14 (1110)	ABT	10110
R13 (1100)	ABT	10111
R8 (1000)	USR, UND, SVC, ABT, IRQ	11000
R9 (1001)	USR, UND, SVC, ABT, IRQ	11001
R10 (1010)	USR, UND, SVC, ABT, IRQ	11010
R11 (1011)	USR, UND, SVC, ABT, IRQ	11011
R12 (1100)	USR, UND, SVC, ABT, IRQ	11100
R13 (1101)	USR	11101
R14 (1110)	USR	11110
Reserved (1111)	ALL	11111

FIG. 5

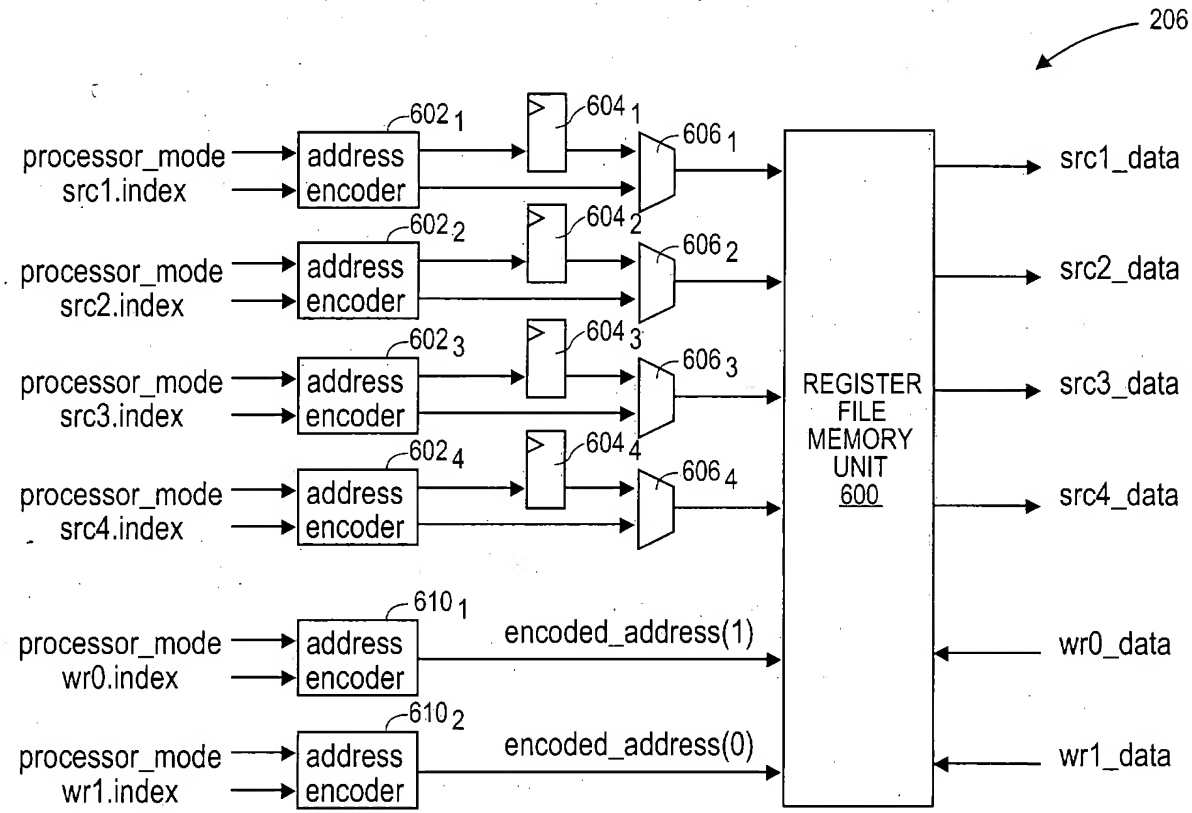
206
processor_mode
src1.index
address
encoder
602 1
604 1
606 1
processor_mode
src2.index
address
encoder
602 2
604 2
606 2
processor_mode
src3.index
address
encoder
602 3
604 3
606 3
processor_mode
src4.index
address
encoder
602 4
604 4
606 4
processor_mode
wr0.index
address
encoder
610 1
encoded_address(1)
processor_mode
wr1.index
address
encoder
610 2
encoded_address(0)
REGISTER
FILE
MEMORY
UNIT
600
src1_data
src2_data
src3_data
src4_data
wr0_data
wr1_data

FIG. 6

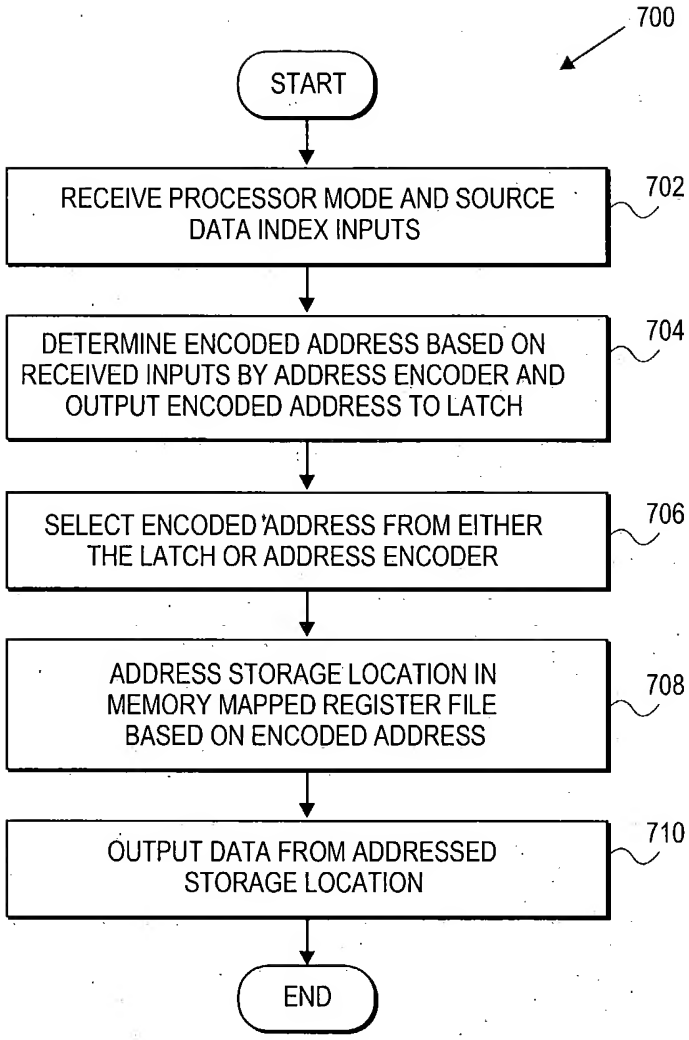
700
START
RECEIVE PROCESSOR MODE AND SOURCE DATA INDEX INPUTS
702
DETERMINE ENCODED ADDRESS BASED ON RECEIVED INPUTS BY ADDRESS ENCODER AND OUTPUT ENCODED ADDRESS TO LATCH
704
SELECT ENCODED ADDRESS FROM EITHER THE LATCH OR ADDRESS ENCODER
706
ADDRESS STORAGE LOCATION IN MEMORY MAPPED REGISTER FILE BASED ON ENCODED ADDRESS
708
OUTPUT DATA FROM ADDRESSED STORAGE LOCATION
710
END

FIG. 7

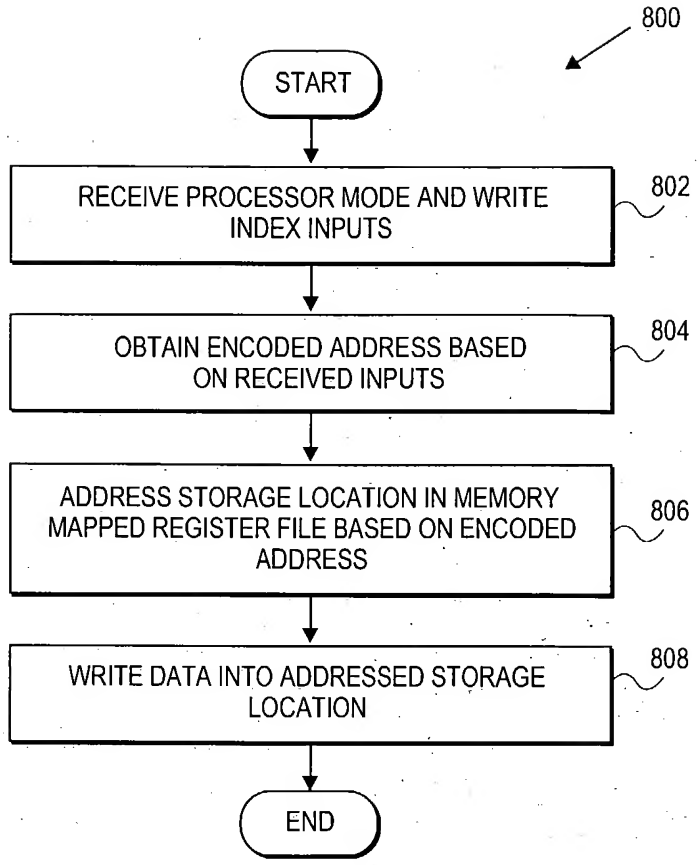
800
START
RECEIVE PROCESSOR MODE AND WRITE INDEX INPUTS
802
OBTAIN ENCODED ADDRESS BASED ON RECEIVED INPUTS
804
ADDRESS STORAGE LOCATION IN MEMORY MAPPED REGISTER FILE BASED ON ENCODED ADDRESS
806
WRITE DATA INTO ADDRESSED STORAGE LOCATION
808
END

FIG. 8